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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,148	12/31/2003	Blaise B. Fanning	42P16958	7922

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EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,148	FANNING, BLAISE B.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-29 are rejected under U.S.C. 102(e) as being anticipated by Olarig et al. (US PGPub 2003/0065886).

Claim 1. A cache memory comprising: *(Title – Claims a Cache Memory)*

- a general-purpose sector, the general-purpose sector to be used for general computer operations; *(Section 0019, lines 1-7 – Claim that the cache can be partitioned. Also, one partition can be assigned a particular bus, which deals with general computer operations)*
- and a dedicated sector, the dedicated sector to be dedicated to a first computer process. *(Section 0019, lines 13-15 – Claim that the dedicated cache partition can be a process)*

Claim 2. The cache memory of claim 1, wherein the dedicated sector is allocated to a first program thread. *(Section 0019, lines 13-15 – Claim that the dedicated cache partition can be a thread)*

Claim 3. The cache memory of claim 2, wherein the first program thread comprises a multi-media process. *(Section 0009, lines 1-10 – Describe the thread as a multi-media process, which is simply a process that utilizes more than one medium)*

Claim 4. The cache memory of claim 1, wherein the dedicated sector may be dynamically created or eliminated. *(Abstract, lines 1-2 – Claim dynamic cache partitioning)*

Claim 5. The cache memory of claim 4, wherein the size of the dedicated sector may be dynamically modified. *(Section 0026, lines 12-14 – Claim that the partition dynamically adapts)*

Claim 6. The cache memory of claim 1, wherein the first computer operation is allocated certain process times. *(Section 0021, lines 1-9 – State the following: "While a partitioned cache represents one form of cache optimization, a partitioned cache can be further optimized by reallocating the sizes of cache partitions based on the activity of the particular cache partitions. One cache statistic that may be useful in identifying cache partitions that are candidates for size reallocation is a moving or running hit average. This cache statistic represents an average number of hits to a cache partition over a particular period of time")*

Claim 7. A processor comprising: (Section 0007, line 7 – Claims a processor)

- a processor core; *(Section 0008, lines 1-2 – Claim that multiple threads and processes may share the cache, which is found on the processor core)*
- a first cache memory for general-purpose operation; *(Section 0019, lines 1-7 – Claim that the cache can be partitioned. Also, one partition can be assigned a particular bus, which deals with general computer operations)*

- and a second cache memory dedicated to a first computer process. *(Section 0019, lines 13-15 – Claim that the dedicated cache partition can be a process)*

Claim 8. The processor of claim 7, wherein first computer process is a multi-media process. *(Section 0009, lines 1-10 – Describe the thread as a multi-media process, which is simply a process that utilizes more than one medium)*

Claim 9. The processor of claim 7, wherein the first computer process is allocated certain computing cycles of the processor. *(Figure 4 – Represents reallocation cycles)*

Claim 10. The processor of claim 7, wherein the first cache memory comprises a first sector of a memory and wherein the second cache memory comprises a second sector of the memory. *(Section 0019, lines 5-7 – State that the memory can be divided into two cache bins)*

Claim 11. The processor of claim 10, wherein the second cache memory may be dynamically created or eliminated. *(Abstract, lines 1-2 – Claim dynamic cache partitioning)*

Claim 12. The processor of claim 10, wherein the size of second cache memory sector may be dynamically modified. *(Section 0026, lines 12-14 – Claim that the partition dynamically adapts)*

Claim 13. A system comprising: *(Figure 1 – Shows a system)*

- a bus; *(Figure 1, Number 160 – Shows a bus)*
- a processor coupled to the bus; *(Figure 1, Numbers 160 and 102 – Show a bus with a processor attached to it)*
- a first cache memory to support general-purpose operation for the processor; *(Section 0019, lines 1-7 – Claim that the cache can be partitioned. Also, one partition can be assigned a particular bus, which deals with general computer operations)*
- and a second cache memory dedicated to a first program thread. *(Section 0019, lines 13-15 – Claim that the dedicated cache partition can be a thread)*

Claim 14. The system of claim 13, wherein first program thread is a multi-media process. *(Section 0009, lines 1-10 – Describe the thread as a multi-media process, which is simply a process that utilizes more than one medium)*

Claim 15. The system of claim 13, wherein the first program thread is allocated certain computing cycles of the processor. *(Figure 4 – Represents reallocation cycles)*

Claim 16. The system of claim 13, wherein the first cache memory comprises a first sector of a memory unit and wherein the second cache memory comprises a second sector of the memory unit. *(Section 0019, lines 5-7 – State that the memory can be divided into two cache bins)*

Claim 17. The system of claim 16, wherein the second cache memory may be dynamically created or eliminated. *(Abstract, lines 1-2 – Claim dynamic cache partitioning)*

Claim 18. The system of claim 16, wherein the size of second cache memory sector may be dynamically modified. *(Section 0026, lines 12-14 – Claim that the partition dynamically adapts)*

Claim 19. The system of claim 13, wherein the first cache memory and the second cache memory are included in the processor. *(Section 0007, lines 9-10 – Claim two caches in the processor)*

Claim 20. A method comprising: *(Claim 1, lines 1 – Declares a method)*

- storing data relating to a plurality of computer operations in a first cache memory; *(Section 0019, lines 1-7 – Claim that the cache can be partitioned. Also, one partition can be assigned a particular bus, which deals with general computer operations)*
- and storing data regarding a first computer process in a dedicated second cache memory. *(Section 0019, lines 13-15 – Claim that the dedicated cache partition can be a process)*

Claim 21. The method of claim 20, further comprising creating the second cache memory. *(Section 0019, lines 5-7 – State that the memory can be divided into two cache bins)*

Claim 22. The method of claim 20, further comprising changing the size of the second cache memory. *(Section 0028, lines 6-10 – Claim that the cache size can be increased or decreased)*

Claim 23. The method of claim 20, further comprising eliminating the second cache memory. *(Section 0032, lines 18-20 - The shrinking of cache partition 400 in Pass 3 shows that a cache partition can be sized so as to eliminate the cache partition altogether)*

Claim 24. The method of claim 20, further comprising flushing the first cache memory without flushing the second cache memory. *(Section 0032, lines 1-3 – State that a particular cache partition is a candidate for losing information)*

Claim 25. A machine-readable medium *(Figure 1 – Shows a machine readable medium)*

- having stored thereon data representing sequences of instructions that, when executed by a processor, cause the processor to perform operations comprising: *(Figures 2, 3 and 5 – Show sequences of instructions)*
- storing data relating to a plurality of computer operations in a first cache memory; *(Section 0019, lines 1-7 – Claim that the cache can be partitioned. Also, one partition can be assigned a particular bus, which deals with general computer operations)*
- and storing data regarding a first computer process in a dedicated second cache memory. *(Section 0019, lines 13-15 – Claim that the dedicated cache partition can be a process)*

Claim 26. The medium of claim 25, wherein the sequence of instructions further comprise instructions causing the processor to perform operations comprising creating the second cache memory. *(Section 0019, lines 5-7 – State that the memory can be divided into two cache bins)*

Claim 27. The medium of claim 25, wherein the sequence of instructions further comprise instructions causing the processor to perform operations

comprising changing the size of the second cache memory. *(Section 0028, lines 6-10 – Claim that the cache size can be increased or decreased)*

Claim 28. The medium of claim 25, wherein the sequence of instructions further comprise instructions causing the processor to perform operations comprising eliminating the second cache memory. *(Section 0032, lines 18-20 - The shrinking of cache partition 400 in Pass 3 shows that a cache partition can be sized so as to eliminate the cache partition altogether)*

Claim 29. The medium of claim 25, wherein the sequence of instructions further comprise instructions causing the processor to perform operations comprising flushing the first cache memory without flushing the second cache memory. *(Section 0032, lines 1-3 – State that a particular cache partition is a candidate for losing information)*

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

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